

WHAT IS CLAIMED IS:

- 1 1. A method of fabricating an integrated circuit, the method
2 comprising:
3 depositing a reflective metal material layer over a layer of
4 polysilicon;
5 depositing an anti-reflective coating over the reflective metal
6 material layer;
7 trim etching the anti-reflective coating to form a pattern;
8 etching the reflective metal material layer according to the
9 pattern; and
10 removing portions of the polysilicon layer using the pattern
11 formed from the removed portions of anti-reflective coating.
- 1 2. The method of claim 1, further comprising depositing a resist
2 layer over the anti-reflective coating;
- 1 3. The method of claim 1, wherein the step of removing
2 portions of the anti-reflective coating comprises providing an isotropic
3 etch to the anti-reflective coating.
- 1 4. The method of claim 1, wherein the reflective metal material
2 layer comprises tungsten.
- 1 5. The method of claim 4, wherein the reflective metal material
2 layer has a thickness of 80-200 Angstroms.
- 1 6. The method of claim 1, wherein a remaining portion of the
2 polysilicon layer is a gate structure.

mark B2

1 7. A method of optimizing optical properties of gate patterning
2 to control gate size in an integrated circuit fabrication process, the
3 method comprising:
4 providing a reflective metal layer over a gate material layer;
5 providing a mask layer over the reflective metal layer; and
6 patterning the gate material layer including selectively
7 etching the mask layer and the reflective metal layer.

mark C1

1 8. The method of claim 7, wherein the reflective metal layer
2 comprises tungsten (W).

mark C2

1 9. The method of claim 7, wherein the patterning step
2 comprises trim etching the mask layer.

mark C3

1 10. The method of claim 7, wherein the reflective metal layer has
2 a thickness of 80-200 Angstroms.

mark C4

1 11. The method of claim 7, wherein the step of providing a mask
2 layer comprises depositing a layer of SiON and a layer of resist.

mark C5

1 12. The method of claim 7, wherein the reflective metal layer is
2 not matched to the gate material layer.

mark C6

1 13. The method of claim 7, wherein the step of providing a
2 reflective metal layer comprises selecting the reflective metal layer based
3 on etch chemistry of the reflective metal layer and the gate material layer.

mark C7

1 14. A method of forming a gate in an integrated circuit, the
2 method comprising:
3 providing a gate material layer;
4 providing a reflective metal layer over the gate material layer;

5 providing an anti-reflective coating (ARC) layer over the
6 reflective metal layer;
7 providing a resist layer over the ARC layer; and
8 patterning a gate structure in the gate material layer by
9 selectively removing portions of the resist layer, ARC layer, and gate
10 material layer.

1 15. The method of claim 14, wherein the reflective material layer
2 comprises tungsten (W).

16. The method of claim 14, wherein the reflective material layer
has a thickness of 100 Angstroms.

1 17. The method of claim 14, wherein the ARC layer comprises
2 SiON.

1 18. The method of claim 14, wherein the step of selectively
2 removing comprises trim etching the ARC layer.

19. The method of claim 18, wherein the ARC layer is SiON.

1 20. The method of claim 19, wherein the reflective metal layer is
2 less than 100 Angstroms thick.